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CLAIMS

[Claim(s)]

[Claim 1] The insulating substrate of the shape of a strip of paper which has two or more pairs of crevices, or heights on the opposite ends edge of the direction of a long side, and has the crevice or heights of a couple on the opposite ends edge of the direction of a shorter side, Two or more electrode terminals formed in the top face of an insulating substrate from the crevice or heights of the edge of this insulating substrate, having covered, The chip mold network resistor equipped with two or more resistance elements formed so that it might lap with two or more electrode terminals formed in the opposite ends edge of the electric conduction line which connects the electrode terminal of the couple formed in the opposite ends edge of the direction of a shorter side, its electric conduction line, and the direction of a long side.

[Claim 2] The chip mold network resistor [equipped with the protective layer which covers two or more resistance elements] according to claim 1.

[Claim 3] The chip mold network resistor according to claim 2 which displayed the delimiter of resistance or a resistance circuit on the protective layer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the chip mold network resistor which has the circuit which consists of two or more electrode terminals and two or more resistance elements linked to them.

[0002]

[Description of the Prior Art] The chip mold network resistor which has eight resistance elements of drawing 6 in the configuration shown in conventional drawing 5 is explained below in order of the process shown in drawing 8. On insulating substrates, such as an alumina with which the slit for dividing into the piece of an individual was generally formed The ** paste and the resistive paste of a ruthenium oxide system are screen-stenciled and elevated-temperature calcinated. conductors, such as silver and palladium, — After forming the resistance circuit which stands in a row considering eight resistance circuits divided to the slit 71 as shown in drawing 7 as a piece of an individual, passivation film, such as glass, is given to the part except an electrode terminal area for stabilization of the pollution control of a resistance element, or the resistance film.

[0003] Then, contacting a probe (probe) to electrode terminals C1, C2, C3, C4, C5, C6,

C7, C8, C9, and C10, and measuring the resistance of resistance elements R1, R2, R3, R4, R5, R6, R7, and R8, trimming by laser etc. is performed to each resistance element, and it is adjusting so that it may become predetermined resistance.

[0004] In order to trim a resistance element R1 in this trimming process when an electrode terminal C1, C1', and C6 and C6' flow and it has become a closed circuit as the dotted line of drawing 7 shows If a probe is contacted to other electrode terminals and the electrical potential difference for surroundings lump prevention of a current is impressed to them while contacting a probe to the electrode terminals C1 and C2 linked to a resistance element R1, measurement and trimming of the resistance element R1 between electrode terminals C [C1 and] 2 will become possible. However, since the equal circuit same about resistance elements R4 and R8 cannot be formed, measurement and trimming of resistance are impossible.

[0005] Therefore, after making open between the electrode terminal C1 shown by the dotted line of drawing 7 , C1', and C6 and C6' and making possible measurement and trimming of resistance elements R4 and R8, trimming is performed about other resistance elements. Then, between an electrode terminal C1, C1', and C6 and C6', conductive paste etc. is printed and calcinated, between them is short-circuited, and a circuit is formed.

[0006] And after ending formation of this connection electrode, the seal 13 of the wrap protective coat 12, resistance, or a resistance circuit delimiter is formed in the top face of an insulating substrate 1 for said resistance circuit.

[0007] On the other hand, after dividing into the piece of an individual the network resistor formed on one alumina substrate, in order to raise the electric conductivity ability and the mounting engine performance (soldering nature) of an electrode terminal, nickel plating and solder plating are performed.

[0008]

[Problem(s) to be Solved by the Invention] However, since the resistance and difference which the trimmed resistance changed and were being made into the object in order to print a connection electrode and to carry out elevated-temperature baking

after resistor trimming by said conventional method of construction between an electrode terminal C1, C1', and C6 and C6' arise and the variation does not become fixed, either, high-degree-of-accuracy-izing of resistance tolerance is difficult.

Moreover, since that which comes outside resistance tolerance may arise when the amount of changes in resistance is large, it is the big factor which influences the process yield.

[0009] This invention has low counts of printing / baking by solving said conventional technical problem and abolishing printing / baking process of a connection electrode, and it aims at moreover offering the good chip mold network resistor of resistance precision and the process yield.

[0010]

[Means for Solving the Problem] In order to attain this object the chip mold network resistor of this invention The insulating substrate of the shape of a strip of paper which has two or more pairs of crevices, or heights on the opposite ends edge of the direction of a long side, and has the crevice or heights of a couple on the opposite ends edge of the direction of a shorter side, Two or more electrode terminals formed in the top face of an insulating substrate from the crevice or heights of the edge of this insulating substrate, having covered, It has two or more resistance elements formed so that it might lap with two or more electrode terminals formed in the opposite ends edge of the electric conduction line which connects the electrode terminal of the couple formed in the opposite ends edge of the direction of a shorter side, its electric conduction line, and the direction of a long side.

[0011]

[Function] By this configuration, since printing and the elevated-temperature baking process of a connection electrode are lost, little resistance precision and process yield of the count of printing / baking can offer a good chip mold resistor network.

[0012]

[Example]

(Example 1) The chip mold network resistor of one example of this invention is

explained below, referring to a drawing. Drawing 1 R> 1 (a) shows the plan of the network resistor in one example of this invention, and drawing 1 (b) and drawing 1 (c) show the side elevation and bottom view of a network resistor which are shown in drawing 1 (a), respectively. Drawing 4 shows process drawing of manufacture of the network resistor in one example of this invention.

[0013] The insulating substrate 11 formed in the shape of a strip of paper in drawing 1 (a), (b), and (c) using the alumina substrate, The common electrode terminals C1 and C6 of the couple formed in the opposite ends edge of the direction of a shorter side of this insulating substrate 11 at the symmetry, The electrode terminals 9 and C [C2, C3, C4, C5, C7, C8, and] 10 formed in the opposite ends edge of the direction of a long side of this insulating substrate 11 at the symmetry, The circuit which consists of the resistance element connected to the electric conduction line 14 which connects the common electrode terminals C1 and C6, and each electrode terminals C2, C3, C4, C5, C7, C8, C9, and C10, respectively The wrap protective coat 12, The chip mold network resistor equipped with the seal 13 which displays resistance on this protective coat 12 is shown. Drawing 2 shows the circuit diagram of the chip mold network resistor shown in drawing 1 .

[0014] In this example, as an insulating substrate 11, 96% as an ingredient of an alumina substrate and the electrode terminal areas C1, C2, C3, C4, C5, C6, C7, C8, C9, and C10 Ag system or Ag/Pd system thick film paste, RuO₂ system thick film paste is used as electrical resistance materials. After screen-stenciling to an insulating substrate 11, It calcinates at a 850-degree C elevated temperature, and the resistance elements R1, R2, R3, R4, R5, R6, R7, and R8 linked to the common electrode terminal areas C1 and C6, the electric conduction line 14 which makes it flow through them, and each electrode terminals C2, C3, C4, C5, C7, C8, C9, and C10 are formed. The resistor network formed on one alumina substrate is shown in drawing 3 . The part divided to the slit 31 in drawing 3 serves as a piece of an individual of the chip mold network resistor shown in drawing 2 .

[0015] In addition, after giving passivation film, such as glass, on the resistance circuit

formed on the insulating substrate 11 after printing baking except for the common electrode terminal areas C1 and C6 and electrode terminals C2, C3, C4, C5, C7, C8, C9, and C10 if needed, in order to adjust resistance, resistance trimming by laser etc. is performed. In this resistance trimming process, if a probe is contacted to other electrode terminals and the electrical potential difference for surroundings lump prevention of a current is impressed to them while contacting a probe to the electrode terminals C1 and C2 linked to a resistance element R1, when trimming a resistance element R1, measurement and trimming of the resistance element R1 between electrode terminals C [C1 and] 2 will become possible. It is possible to carry out by technique with the same said of the trimming of other resistance elements.

[0016] After trimming termination, for a wrap reason, a glass paste or a resin paste is printed for the resistance circuit formed on the insulating substrate 11 as a protective coat 12, and a resistance circuit is protected. And after forming a protective coat 12, the seal 13 of resistance or a resistance circuit delimiter is displayed. In addition, since a resin paste can harden in a low-temperature process, the process variation of resistance can be stopped small and high-degree-of-accuracy-ization of resistance tolerance can be attained more.

[0017] Then, after dividing into the piece, of an individual the network resistor formed in the shape of a sheet, in order to raise the electric conductivity ability and the mounting engine performance (soldering nature) of an electrode terminal, nickel plating and solder plating are performed.

[0018] Since it is [that what is necessary is just to carry out printing formation of a glass paste or the resin paste for the resistance circuit formed on the insulating substrate 11 as a protective coat 12 for a wrap reason, and to display the seal 13 of ~~resistance or a resistance circuit delimiter after that after resistance trimming~~]

unnecessary in the process which connects a common electrode according to this example as mentioned above while it becomes unnecessary to prepare an electrode opening part before resistance trimming like before, printing manday can be reduced. Moreover, since the resistance value change produced at the time of

elevated-temperature baking of the conventional connection electrode is also lost, while being able to attain high-degree-of-accuracy-ization of resistance tolerance, since resistance value distribution becomes good according to the effectiveness, the process yield also improves.

[0019] In addition, although it has concave electrode terminal structure in this example as shown in drawing 1, it is clear that the same effectiveness is acquired also with convex type electrode structure.

[0020] (Example 2) In the circuit of the network resistor shown in drawing 2 of an example 1, in the case of the parallel circuit which makes all resistance the same, since the common electrode terminals C1 and C6 are arranged at the symmetry on the opposite ends edge of the direction of a shorter side of an insulating substrate 11, mounting directivity is lost, and it also becomes preventing a mounting mistake.

[0021]

[Effect of the Invention] The insulating substrate of the shape of a strip of paper which this invention has two or more pairs of crevices, or heights on the opposite ends edge of the direction of a long side, and has the crevice or heights of a couple on the opposite ends edge of the direction of a shorter side as mentioned above, Two or more electrode terminals formed in the top face of an insulating substrate from the crevice or heights of the edge of this insulating substrate, having covered, By having two or more resistance elements formed so that it might lap with two or more electrode terminals formed in the opposite ends edge of the electric conduction line which connects the electrode terminal of the couple formed in the opposite ends edge of the direction of a shorter side, its electric conduction line, and the direction of a long side Printing and the elevated-temperature baking process of a connection electrode are lost, there are few counts of printing / baking, and resistance precision and the process yield can offer a good chip mold resister network.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] (a) The plan of the chip mold network resistor in the 1st example of this invention

(b) The side elevation of this chip mold network resistor

(c) The bottom view of this chip mold network resistor

[Drawing 2] The circuit diagram of this chip mold network resistor

[Drawing 3] The circuit diagram on the alumina substrate of this chip mold network resistor

[Drawing 4] Process drawing of manufacture of this chip mold network resistor

[Drawing 5] The plan of the conventional chip mold network resistor

[Drawing 6] The circuit diagram of this chip mold network resistor

[Drawing 7] The circuit diagram on the alumina substrate of this chip mold network resistor

[Drawing 8] Process drawing of manufacture of this chip mold network resistor

[Description of Notations]

11 Insulating Substrate

12 Protective Coat

13 Seal Which Shows Resistance

14 Electric Conduction Line

31 Slit

C1-C10 Electrode terminal

C1 (C1'), C6 (C6') Common electrode terminal

R1-R8 Resistance element

[Translation done.]

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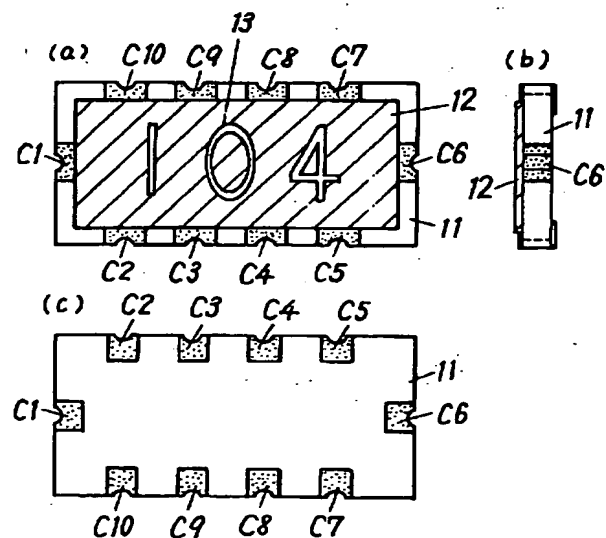
(54) 【発明の名称】 チップ型ネットワーク抵抗器

(57) 【要約】

【目的】 チップ型ネットワーク抵抗器において、抵抗値トリミング後の接続電極印刷・焼成工程をなくすことにより、印刷・焼成回数が少なく、しかも抵抗値精度と工程歩留りを向上を図ることを目的とする。

【構成】 長辺方向の対向両端縁に複数対の凹部または凸部を有し短辺方向の対向両端縁に一对の凹部または凸部を有する短冊状の絶縁基板11と、この絶縁基板11の端縁の凹部または凸部から絶縁基板11の上面にかけて形成された複数の電極端子C2～C5、C7～C10と、短辺方向の対向両端縁に形成された一对の電極端子C1、C6をつなぐ導電線と、その導電線と長辺方向の対向両端縁に形成された複数の電極端子C2～C5、C7～C10に重なるように形成された抵抗素子R1～R8と、その抵抗回路を被覆する保護層12を備えた構成としたものである。

11 絶縁基板
12 保護膜
13 捺印



【特許請求の範囲】

【請求項1】 長辺方向の対向両端縁に複数対の凹部または凸部を有し短辺方向の対向両端縁に一对の凹部または凸部を有する短冊状の絶縁基板と、この絶縁基板の端縁の凹部または凸部から絶縁基板の上面にかけて形成された複数の電極端子と、短辺方向の対向両端縁に形成された一对の電極端子をつなぐ導電線と、その導電線と長辺方向の対向両端縁に形成された複数の電極端子に重なるように形成された複数の抵抗素子を備えたチップ型ネットワーク抵抗器。

【請求項2】 複数の抵抗素子を被覆する保護層を備えた請求項1記載のチップ型ネットワーク抵抗器。

【請求項3】 抵抗値または抵抗回路の識別記号を保護層上に表示した請求項2記載のチップ型ネットワーク抵抗器。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は複数の電極端子と、それらに接続する複数の抵抗素子から成る回路を有するチップ型ネットワーク抵抗器に関するものである。

【0002】

【従来の技術】従来の図5に示す形状で図6の8素子の抵抗素子を有するチップ型ネットワーク抵抗器について、図8に示す工程順に以下説明する。一般に、個片に分割するためのスリットが形成されたアルミナ等の絶縁基板上に、銀・パラジウム等の導体用ペーストと酸化ルテニウム系の抵抗ペーストをスクリーン印刷・高温焼成し、図7に示すようなスリット71で区切られた8素子の抵抗回路を個片として連なっている抵抗回路を形成した後、抵抗素子の汚染防止や抵抗膜の安定化のため、電極端子部を除いた部分にガラスなどのパッシベーション膜を施す。

【0003】その後、電極端子C1、C2、C3、C4、C5、C6、C7、C8、C9、C10にプローブ（探針）を接触させて抵抗素子R1、R2、R3、R4、R5、R6、R7、R8の抵抗値を測定しつつ、各々の抵抗素子にレーザー等によるトリミングを実行し、所定の抵抗値になるように調節している。

【0004】このトリミング工程において、図7の点線で示すように電極端子C1とC1'、C6とC6'が導通して閉回路になっている場合に、抵抗素子R1をトリミングするには、抵抗素子R1に接続する電極端子C1、C2にプローブを接触させると共に、他の電極端子にもプローブを接触させて電流の回り込み防止のための電圧を印加すれば、電極端子C1とC2間の抵抗素子R1の測定・トリミングが可能となる。しかし、抵抗素子R4、R8については同様な等価回路が形成できないため、抵抗値の測定とトリミングは不可能である。

【0005】そのため、図7の点線で示した電極端子C1とC1'、C6とC6'の間をオープンにして、抵抗

素子R4、R8の測定・トリミングを可能にしたうえで、他の抵抗素子についてもトリミングを行う。その後、電極端子C1とC1'、C6とC6'の間に導電ペースト等を印刷・焼成して、それらの間を短絡して回路を形成する。

【0006】そしてこの接続電極の形成を終了した後、絶縁基板1の上面に前記抵抗回路を覆う保護膜12と抵抗値または抵抗回路識別記号の捺印13を形成する。

【0007】他方、1枚のアルミナ基板上に形成されたネットワーク抵抗器を個片に分割した後、電極端子の電気導通性能と実装性能（はんだ付け性）を向上させるため、ニッケルめっき・はんだめっきを施す。

【0008】

【発明が解決しようとする課題】しかしながら前記従来の工法では、抵抗トリミング後に電極端子C1とC1'、C6とC6'の間に接続電極を印刷し高温焼成するために、トリミングした抵抗値が変化して目的としていた抵抗値と差が生じ、その変化量も一定にならないため、抵抗値許容差の高精度化が難しい。また、抵抗値変化量が大きいたまには、抵抗値許容範囲外になるものが生じる可能性もあるため、工程歩留りを左右する大きな要因となっている。

【0009】本発明は前記従来の課題を解決するもので、接続電極の印刷・焼成工程をなくすことにより、印刷・焼成回数が少なく、しかも抵抗値精度と工程歩留りの良いチップ型ネットワーク抵抗器を提供することを目的とする。

【0010】

【課題を解決するための手段】この目的を達成するために本発明のチップ型ネットワーク抵抗器は、長辺方向の対向両端縁に複数対の凹部または凸部を有し、短辺方向の対向両端縁に一对の凹部または凸部を有する短冊状の絶縁基板と、この絶縁基板の端縁の凹部または凸部から絶縁基板の上面にかけて形成された複数の電極端子と、短辺方向の対向両端縁に形成された一对の電極端子をつなぐ導電線と、その導電線と長辺方向の対向両端縁に形成された複数の電極端子に重なるように形成された複数の抵抗素子を備えている。

【0011】

【作用】この構成によって、接続電極の印刷・高温焼成工程がなくなるので、印刷・焼成回数の少ない、抵抗値精度と工程歩留りが良いチップ型抵抗ネットワークを提供することができる。

【0012】

【実施例】

（実施例1）以下本発明の一実施例のチップ型ネットワーク抵抗器について、図面を参照しながら説明する。図1(a)は本発明の一実施例におけるネットワーク抵抗器の上面図を示し、図1(b)と図1(c)はそれぞれ図1(a)に示すネットワーク抵抗器の側面図と下面図

を示す。図4は本発明の一実施例におけるネットワーク抵抗器の製造の工程図を示す。

【0013】図1(a), (b), (c)において、アルミナ基板を用いて短冊状に形成した絶縁基板11と、この絶縁基板11の短辺方向の対向両端縁に対称に形成した一对の共通電極端子C1, C6と、この絶縁基板11の長辺方向の対向両端縁に対称に形成した電極端子C2, C3, C4, C5, C7, C8, C9, 10と、共通電極端子C1とC6をつなぐ導電線14と各電極端子C2, C3, C4, C5, C7, C8, C9, C10とにそれぞれ接続される抵抗素子から成る回路を覆う保護膜12と、この保護膜12上に抵抗値を表示する捺印13とを備えたチップ型ネットワーク抵抗器を示している。図2は図1に示されたチップ型ネットワーク抵抗器の回路図を示している。

【0014】本実施例では、絶縁基板11として96%アルミナ基板、電極端子部C1, C2, C3, C4, C5, C6, C7, C8, C9, C10の材料としてAg系またはAg/Pd系厚膜ペースト、抵抗材料としてRuO₂系厚膜ペーストを用い、絶縁基板11にスクリーン印刷の後、850℃の高温で焼成して共通電極端子部C1, C6とそれらを導通させる導電線14と各電極端子C2, C3, C4, C5, C7, C8, C9, C10に接続する抵抗素子R1, R2, R3, R4, R5, R6, R7, R8を形成している。1枚のアルミナ基板上に形成された抵抗回路網を図3に示す。図3においてスリット31で区切られた部分が、図2に示すチップ型ネットワーク抵抗器の個片となる。

【0015】なお、必要に応じて共通電極端子部C1, C6と電極端子C2, C3, C4, C5, C7, C8, C9, C10を除いて、印刷焼成後に絶縁基板11上に形成された抵抗回路上にガラスなどのパッシベーション膜を施した後に、抵抗値を調整するためレーザー等による抵抗値トリミングを行う。この抵抗値トリミング工程において、例えば抵抗素子R1をトリミングする場合は抵抗素子R1に接続している電極端子C1, C2にプローブを接触させると共に、他の電極端子にもプローブを接触させて電流の回り込み防止のための電圧を印加すれば、電極端子C1とC2間の抵抗素子R1の測定・トリミングが可能となる。他の抵抗素子のトリミングについても同様の手法によって行うことが可能である。

【0016】トリミング終了後、絶縁基板11上に形成された抵抗回路を覆うため保護膜12としてガラスペーストもしくは樹脂ペーストを印刷して抵抗回路を保護する。そして、保護膜12を形成した後、抵抗値または抵抗回路識別記号の捺印13を表示する。なお、樹脂ペーストの方が低温プロセスで硬化できるので、抵抗値の工程変化量を小さく抑えることができ、より抵抗値許容差の高精度化を図ることができる。

【0017】この後、シート状に形成されたネットワー

ク抵抗器を個片に分割した後、電極端子の電気導通性能と実装性能(はんだ付け性)を向上させるため、ニッケルめっき・はんだめっきを施す。

【0018】以上のように本実施例によれば、従来のように抵抗値トリミング前に電極オープン部分を設ける必要がなくなると共に、抵抗値トリミング後には、絶縁基板11上に形成された抵抗回路を覆うため保護膜12としてガラスペーストもしくは樹脂ペーストを印刷形成して、その後に抵抗値または抵抗回路識別記号の捺印13を表示するだけでよく、共通電極を接続する工程が必要ないので、印刷工数が低減できる。また、従来の接続電極の高温焼成時に生じていた抵抗値の変化もなくなるので、抵抗値許容差の高精度化が図れると共に、その効果によって抵抗値分布が良くなるので工程歩留りも向上する。

【0019】なお、この実施例では図1に示すように凹型電極端子構造となっているが、凸型電極構造でも同様の効果が得られるのは明白である。

【0020】(実施例2) 実施例1の図2に示すネットワーク抵抗器の回路において、全ての抵抗値を同じとする並列回路の場合、共通電極端子C1, C6が絶縁基板11の短辺方向の対向両端縁に対称に配置されるので実装方向性がなくなり、実装間違いを防ぐことにもなる。

【0021】

【発明の効果】以上のように本発明は、長辺方向の対向両端縁に複数対の凹部または凸部を有し、短辺方向の対向両端縁に一对の凹部または凸部を有する短冊状の絶縁基板と、この絶縁基板の端縁の凹部または凸部から絶縁基板の上面にかけて形成された複数の電極端子と、短辺方向の対向両端縁に形成された一对の電極端子をつなぐ導電線と、その導電線と長辺方向の対向両端縁に形成された複数の電極端子に重なるように形成された複数の抵抗素子を備えることにより、接続電極の印刷・高温焼成工程がなくなり、印刷・焼成回数が少なく、抵抗値精度と工程歩留りが良いチップ型抵抗ネットワークを提供することができるものである。

【図面の簡単な説明】

【図1】(a) 本発明の第1の実施例におけるチップ型ネットワーク抵抗器の上面図

(b) 同チップ型ネットワーク抵抗器の側面図

(c) 同チップ型ネットワーク抵抗器の下面図

【図2】同チップ型ネットワーク抵抗器の回路図

【図3】同チップ型ネットワーク抵抗器のアルミナ基板上の回路図

【図4】同チップ型ネットワーク抵抗器の製造の工程図

【図5】従来のチップ型ネットワーク抵抗器の上面図

【図6】同チップ型ネットワーク抵抗器の回路図

【図7】同チップ型ネットワーク抵抗器のアルミナ基板上の回路図

【図8】同チップ型ネットワーク抵抗器の製造の工程図

【符号の説明】

- 11 絶縁基板
12 保護膜
13 抵抗値を示す捺印
14 導電線

* 31 スリット

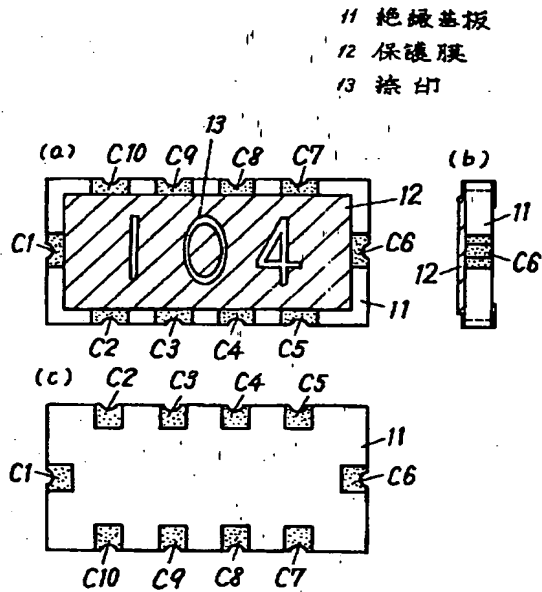
C1~C10 電極端子

C1 (C1'), C6 (C6') 共通電極端子

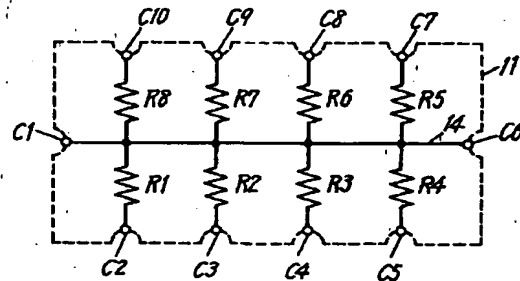
R1~R8 抵抗素子

*

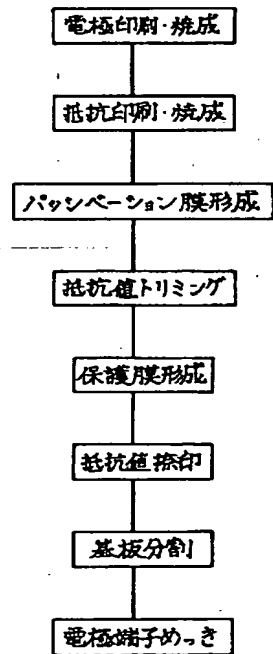
【図1】



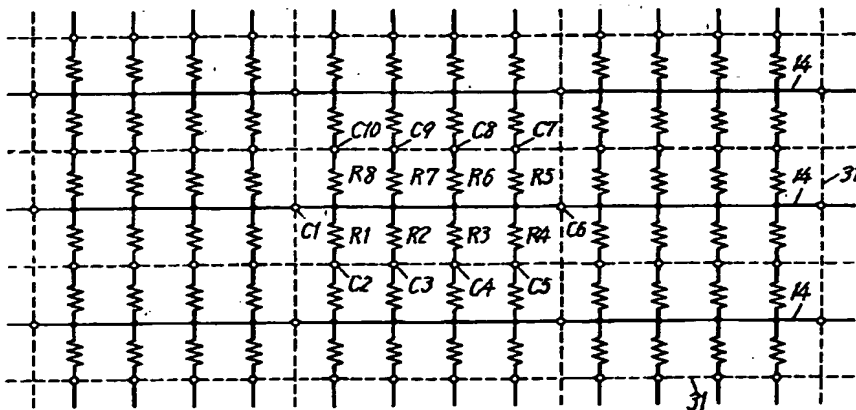
【図2】



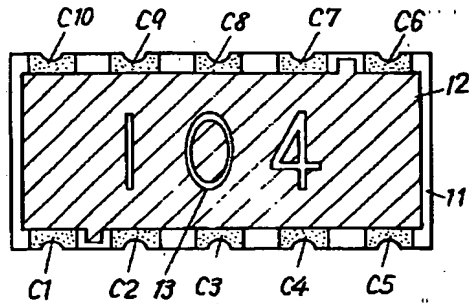
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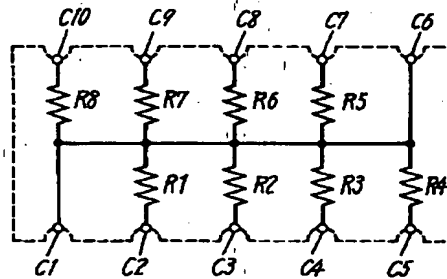
【図3】



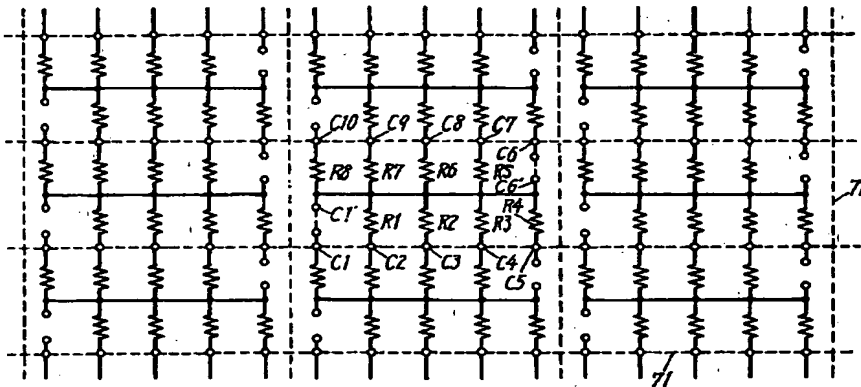
【図5】



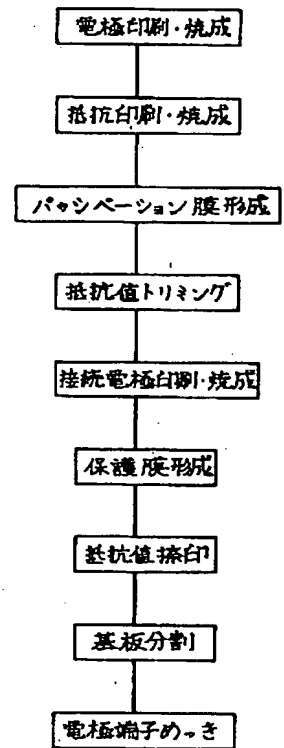
【図6】



【図7】



【図8】



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